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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,742	12/31/2001	Sushma Shrikant Trivedi	4860.P2691	3350

7590	04/03/2006	**EXAMINER**

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EXAMINER
PAN, DANIEL H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*10 January 2006*</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>*1-71*</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>*1-71*</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>*31 December 2001*</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

1.   Claims 1- 71 remain for examination.

2.   Applicant's arguments with respect to claims 1-70 have been considered but are moot in view of the new ground(s) of rejection. New references Morton (5,822,606) in view of Chin et al. (5,497,465) have been introduced to show the newly amended feature of the single chipset.

3.   However, response to applicant's remark in regard to Beard (5,430,884), which is used to show some features of dependent clams ,will be addressed below to clarify the issue.

4.   In the remark, applicant argued that :

5.   a) Beard is part of host processor, not as part of chipset that interface (e.g. the north bridge) the host processors and the rest of the components:

6.   As to a) above, Morton has been introduced to show the chipset (see action below). Although Beard taught the processors part of the host, it could be implemented in a chip setting. One of ordinary skill in the art should be able recognize the vector and scalar in Beard could be applicable in a chip in general . As to the north bridge, applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite a north bridge.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims   1-4 ,10, 12,13   19-29,   33 , 37-39,   40-45, 49, 53-61, 65, 70,71

are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton (5,822,606)

in view of Chin et al. (5,497,465).

8.   Morton taught   an apparatus in an integrated circuit (IC) of a data processing

system (see fig.1) , comprising:

a) a chip interconnect (see buses 117, 108, 128 , 109 in the chip);

b) a memory controller (see memory interface 101) for controlling the host memory

comprising DRAM memory (see how memory interface configured to operate on high

speed DRAMs in col.10, lines 30-17), the memory controller [101] coupled to the chip

interconnect   (see 101 at the input port in fig.1);

c) a scalar processing unit (107) coupled to the chip interconnect, the scalar processing

unit being capable of executing instructions to perform scalar data processing',

d) a vector processing unit (see 110-113, see also fig.10 for detailed structure of vector

processor) coupled to the chip interconnect, the vector processing unit being capable

of executing instructions to perform vector data processing; and

an input and output (1/0) interface (see Parallel I/O with connected buffer ports and the

buses) coupled to the chip interconnect, the V0 interface receiving/transmitting data

from/to the scalar and/or vector processing units a wherein the chip interconnect (SEE

THE BUSES) the memory controller [101] the scalar processing unit [107] the vector

processing units [110-113] and the 1/0 interface [I/O] are implemented within the IC

which is a single chipset (see fig.1, see the single DSP chip in col.9, lines 28-56).

9.   . Morton did not specifically teach the single chipset was interfacing a host as

claimed . However, Chin disclosed a system including a vector and scalar

processing interfacing with a host (see fig.1, host 24). It would have been obvious to

one of ordinary skill in the art to use Chin in Morton for including the host as clamed

because the use of Chin could provide Morton the ability to expand the communicate

path of the vector and scalar processors, therefore, increasing the system processing

capability and the connectivity, and it could be readily achieved by redefining the host of

Chin into the configuration file of Morton with modified control parameter, such as the

read/write port of the host so that the host Chin could   be recognized by Morton, and

because Morton also taught an external memory interfaced with the chip set for

receive fast speed transfer (see col.9, lines 60-64, col.10, lines 30-17), which was a

suggestion of the need for adapting to a fast external device such as host processor,

or the like, in order to increase the processing   efficiency, and therefore, provided a

motivation.

10.   As to clams 24, 40, 56, Morton also taught :

a) receiving data stream from an input/output (IO) interface coupled to the chip

interconnect (see the I/O data in col.10, lines 60-67, col.col.11, lines 1-24, lines 25-59);

b) examining data of the data stream to determine whether the data requires scalar

data processing or vector data processing (see instruction to specify the scalar

processing and vector processing in col.18, lines 1-12, see also the crossbar switch in

col.22, lines 31-60);

c) performing scalar data processing on the data in the IC, if the data ' requires scalar

data processing (see col.22, lines 52-55); and

d) performing vector data processing on the data in the IC, if the data required vector

data processing wherein receiving the data streams examining the data (see col.22,

lines 42-47, lines 23, lines 7-14) .

11.   Morton did not specifically teach the single chipset was interfacing a host as

claimed . However, Chin disclosed a system including a vector and scalar

processing interfacing with a host (see fig.1, host 24). It would have been obvious to

one of ordinary skill in the art to use Chin in Morton for including the host as clamed.

The reasons of obviousness have been given in paragraph # 5 , therefore, it will not be

repeated herein.

12.   As to claims 2, 27,28, 43, 44, 57, 58, 59, 60,   Morton also included the switch

mechanism for receiving or dispatching the data streams (see the crossbar for

transmitting and receiving data in col.22, lines 31-67, col.23, lines 1-19, see the reading

of the data cache and the crossbar in col.23, lines 20-64).

13.   AS to claims 3, 4, 25, 26, 41, 42, Morton also included processing instructions

in multiple scalar units and multiple vector units simultaneously , and one of a kind

(see the parallel chips in col.13, lines 50-67).

14.   AS to claim 10, Morton also included VLIW (see col.2,lines 38-40).

15.   As to claims 12,13, 33, 49, 65, Morton also included shift unit , the integer and

floating point (see the shift instructions in col.20, lines 51-56, cool.35, lines 50-60, see

the integer in col.40, lines 1-2, see floating point in col.2, lines 25-29).

16.   As to claims 19,37, 53, 59, Morton also included asynchronous data processing

(see col.6, lines 50-55).

17.   AS to claims 20, 38,54, 70,   Morton also included interrupt processing (see

interrupt controller in col.9, lines 60-65).

18.   As to claims 21, 39, 55, 71, Morton did not explicitly show the memory mapped

addresses as clamed. However, Morton in the same patent taught interface with

external memory with DMA (see col.9, lines 60-67), and since the difference in size

with the external memory ,   it must have a memory mapped space in order to perform

the DMA operation.

19.   As to claim 22, Morton's IC was a coprocessor (see DSP chip).

20.   AS to claim 23, Morton also included a special propose file (see the real time

applications in col.6, lines 64-65).

21.   As to claims 29,45, 61, Morton also included encoding instruction (see decoder

in col.13, lines 20-22, see also instruction decoder in col.17, lines 40-53).

22.   Claims 5-9, 11, 30-32, 46, 47, 48, 62, 63,64 are rejected under 35

U.S.C. 103(a) as being unpatentable over Morton (5,822,606) in view of Chin et al.

(5,497,465) as applied to claims 1-4 ,24,40, 56 above, and further in view of Beard

(5,430,884) .

23.   As to claims 5,30,46,62,   Morton also included :

a) general purpose registers (see scalar registers in fig.6. 604);

b) vector registers (see vector registers in fig.10).

Morton nor Chin specifically showed the load and store unit as claimed,. However

Beard taught a load and store unit (LSU), the LSU being capable of executing

instructions to load and store scalar data from and to the GPR, and the LSU being

capable of executing instructions to load and store vector data from and to the VR (see

f1g.17, load request and store request, see also col.30, lines 65-67).

It would have been obvious to one of ordinary skill in the art to use Beard in Morton for

including the load and store unit as claimed because the use of Beard could provide

Morton the capability to load and store data in the memory cache in response to a

predetermined read/write command, such as load an or store, therefore, provide the

access of the memory based on specific command defined by sty tem.

24.   As to claims 6, 31, 47, 63, Beard taught loads and stores data from and to the

memory

location (see memory location in fig.17).

25.   As to claims 7, 32,48,64, Morton also included a DMA (see DMA controller in

col.12 lines 40-57).

26.   As to claim 8, Morton also included 8 bit and 16 bit (see col.12, lines 40-57).

Beard also included bit length up to 32 (see col.7, lines 60-65).

27.   As to claim 9, Beard also included dispatch unit (see instructions dispatch in

col.29, lines 57-60).

28.   As to claim 11, neither Morton nor Chin specifically showed the branch unit as

claimed. However, Beard   taught a branch unit, wherein the program counter and the

branch unit determine the location to fetch next instructions (see fig.1 branch unit). It

would have been obvious to one of ordinary skill in the art to use Beard in Morton for

including the branch unit as clamed because the   use of Beard could provide Morton

the ability to process the instructions out of a normal sequence, thereby increasing the

look ahead execution control of the instructions , and one ordinary skill in the art should

be able to recognize the teaching of parallel instructions processing in Morton would

have suggested the use of out-of 0sequence processing , such as a branch in order to

increasing the processing efficiency, and for doing provided a motivation.

29.   Claims 14-18, 34-36, 50-52 , 66-68   are rejected under 35 U.S.C. 103(a) as

being unpatentable over Morton (5,822,606) in view of Chin et al. (5,497,465) as

applied to claim 1,24, 40 ,56,   and further in view of Dowling (6,597,745).

30.   As to claims 14,34, 50,66,   Morton did not specifically show the vector

permutation, or the complex integer as clamed. However, Dowling taught system

including a vector permutation (see col.13, lines 55-62) and complex integer (see

complex integer in col.4, lines 1-8). It would have been obvious to one of ordinary skill

in the art to use Dowling in Morton for including the vector permutation and complex

integer as claimed because the use of Dowling could provide Morton the ability to

accept more complex data calculation (e.g. vector permuting and integer addition with

multiply etc.), thereby expanding the processing capability of Morton, and because

Morton did disclose a multiplicity of add , shit and logical operations (see col.35, lines

10-60), which was a suggestion of the need for including the a more complex arithmetic

operations, such as vector permutation complex integer, for reducing the latency I the

parallel processing.

31.   As to claims 15, Morton also included vector floating point (see floating pint in

col.2,lines 38-40).

32.   As to claims 16, 35,51,67,   Morton also included lookup table (see col.31, lines

5-14).

33.   As to claims 17, 36, 52, 68,   Morton also included DMA (see DMA in col.10, lines

51-67

34.   As to claim18, Morton also included SRAM (see col.11, lines 25-27).

Applicant's amendment necessitated the new ground(s) of rejection presented in .

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from

8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is

assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the

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21 Century   Strategic   Plan

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